Effective ways of testing parallel BER on 2.5Gps high-speed interface devices

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This presentation addresses the parallel BER testing needs on electrical interfaces of devices in R&D and manufacturing.

It is continuation of another presentation held a year ago focussing on test needs of MUX/DEMUX devices [1]. Today we review this again but also take a look into the test needs of multiple serial devices.

The test methods discussed in this presentation leverage a number of newly developed technologies to achieve a major boost in test performance and efficiency.

This presentation focuses on:

- the fundamentals of parallel BER testing
- how the parallel test method makes testing more efficient in R&D and manufacturing
- the efficiency is also a matter of the visualization, here we will look on the results gathered from a Gigabit Ethernet Chip.

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- High Speed Devices using Mux/Demux/Parallel Technology, the Mux/Demux Architecture
- Test Requirements of a Gigabit Ethernet Chip and a Multiple Serial Optical Transceiver
- Today's testing in R&D and Manufacturing
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- The Fast Eye Mask Measurement
- Test Results from a Gigabit Ethernet Chip

During this presentation:

•We will talk about:

•high speed devices using MUX/DEMUX/parallel technology

•The generic architecture of MUX/DEMUX devices

•the test requirements of a Gigabit Ethernet chip and of multiple serial optical transceivers

•today's testing in R&D and manufacturing and the better way of using the parallel test technology

•Then we will discuss how to make timing measurements using the parallel technology.

We will look at the implementation of the 'fast eye mask' measurement for manufacturing.

•Finally we will have a look to the visualization of measurement results taken from a Gigabit Ethernet chip

High Speed Interfaces

Using Mux/Demux/Parallel Technology

Local Area Networks

- Gigabit Ethernet
- Fiber Channel
- InfiniBand
- Storage Area Networks
- serial speed: 2.5GBit/s
- MUX 1:10

Digital Video

- HDTV
- Display Links
- Flat Panel
- serial speed 1.5GBit/s
- MUX 1:7

Global Networks

- Terrestrial
- SONET/SDH
- Undersea
- serial speed 10GBit/s, future 40GBit/s
- MUX 1:4, 1:6

Components

- Backplane Serializer/ De-Serializer
- Multiple serial E/O, O/E
- serial speed up to 2.5GBit/s

Agilent Technologies

MUX/DEMUX parts are essential to communication technology. These parts transmit and receive data over electrical or optical transmission links.

MUX/DEMUX components are used in:

- **Local area networks,**
- **Digital video, and**
- **Global networks.**

Within local area networks, **the applications are:**

- **Gigabit Ethernet, Fiber Channel, Infiniband, and Storage Area Networks.**

These applications use a serial speed of 2.5 GBit/s with a typical MUX ratio of 1:10

The digital video **applications are:**

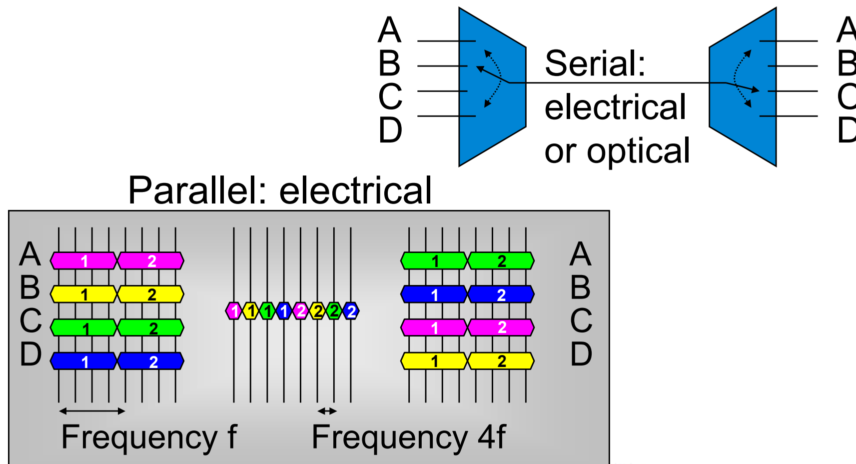
- **HDTV, Display Links, and Flat Panel Interfaces.**

Today, serial speeds can reach 1.5 GBit/s with a MUX ratio of 1:7.

The total bandwidth of these links is often much higher. However, that is a result of combining several serial lines.

Global networks **using SONET / SDH protocol are terrestrial or undersea.**

The serial speed is currently 10 GBit/s with a future potential speed of 40 GBit/s. The typical MUX ratio is 1:4 and 1:16.



MUX/DEMUX parts collect and distribute data that is transmitted over electrical or optical links.

The transmitter (TX) collects information from a number of parallel lines and, supported by MUX circuitry, puts it on a fast serial line. Speeds on the serial line can reach 1:4, 1:7, 1:10 1:20 compared to parallel lines.

The receiver (RX) side, using DEMUX circuitry, receives the high-speed data and moves it to a parallel bus so that ASIC protocol can process it at a slower speed.

This slide shows an example of a 1:4 implementation. Note that the frequency is 4 times faster on the serial side.

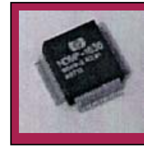
This simple picture does not take into account any complicated latency issues. However, be aware that on the receiver side the parallel data may undergo a cyclic shift.

Test Requirements

Gigabit Ethernet Chip

- HDMP-2634 from

Agilent Technologies



Functional Description:

- Single bipolar circuit with TX and RX
- QFP package, 64 pin
- Low-cost physical layer solution, up to 2.5 GBit/s
- 10-bit wide for 8B/10B coding
- Receiver synchronizes on the ‘comma’ character

Fiber Channel / Gigabit Ethernet Implementation (1)

There are silicon, bipolar, and integrated transceivers on the market from several vendors.

This presentation focuses on Agilent’s HDMP-2634 chip. This chip comes in a 64-pin QFP package as a low-cost physical layer solution.

- Both serializer and de-serializer components are contained in the same package.

- The parallel side is 10-bits wide for 8B/10B coding.

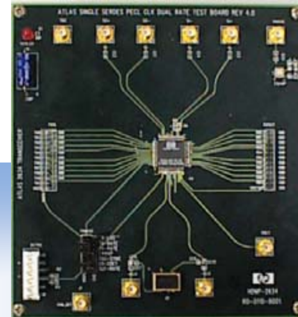
- The receiver synchronizes the parallel outputs on the ‘comma’ character.

Test Requirements

Gigabit Ethernet Evaluation Board

- HDMP-2634 from

Agilent Technologies



Design Issues:

- BER
- Eye Opening
- Input/Output Timing
- Input sensitivity (Demux)
- Jitter (Mux)

Fiber Channel / Gigabit Ethernet Implementation (2)

This is the chip mounted on an Evaluation board. The design issues (also points for the data sheet) are:

- **BER**
- **Eye opening**
- **Input / output timing**
- **Input sensitivity (DEMUX)**
- **Jitter (MUX out)**

Test Requirements

Multiple Serial Optical Transceiver

Multiple Serial
electrical Out
@ 2500 Mbit/s

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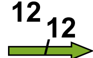

Multiple Serial
electrical In
@ 2500 Mbit/s

Design Issues:

- BER
- Eye Opening

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<u>This is a Multiple Serial Optical Transceiver</u>

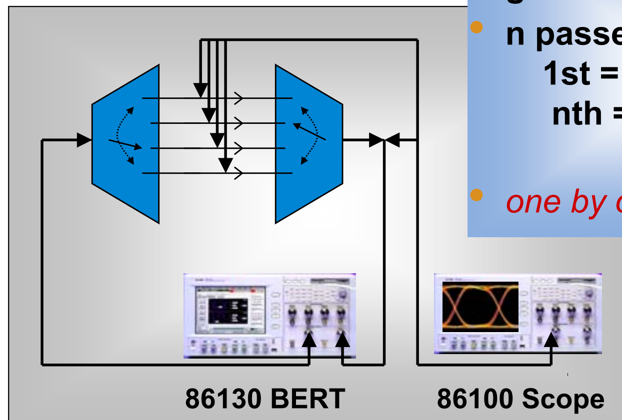
On the electrical side the design issues are:

- **BER**
- **Eye opening**

Today’s Testing

(Mux/) Demux

- Loop-back, Mux is the golden device for Demux
- n passes
  1st = BER
  nth = Timing / Eye Opening
- *one by one*



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This is today’s scenario to test a DEMUX:

The traditional Bit Error Rate test method needs a golden device. So the DEMUX can’t be tested without a MUX (and vice versa)

•A golden device inverts the DUT functionality. Using a golden device means testing can be achieved between similar interfaces. However, maintaining a golden device is a costly issue. It is not easy to maintain its precision or to assure that it does not become marginal.

Second is the ‘timing measurement’ on the parallel side of the DEMUX: In this case a scope will be used to check output by output in reference to the clock.

Inherent disadvantages of this method:

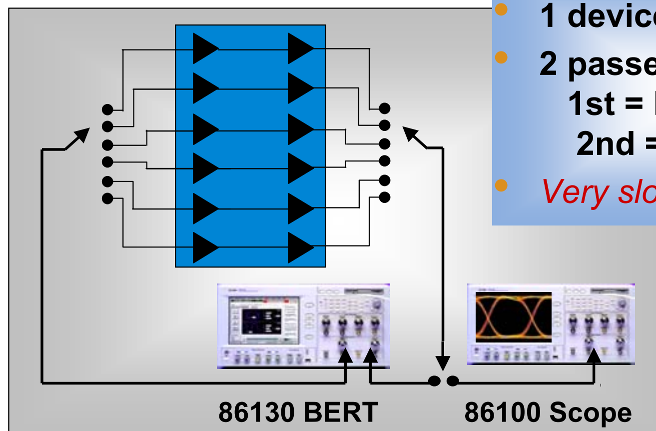
•Slow because of the n-pass approach.

Verdict:

OK for R&D lab use, but far too slow and cumbersome for manufacturing applications.

Today's Testing

Multiple Optical Transceiver



- 1 device at a time
- 2 passes
  1st = BER
  2nd = Eye Opening
- *Very slow*

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Here we look on the electrical interface, assuming he optical side is looped.

The traditional Bit Error Rate test method checks "one channel at a time" in two passes: A high-speed BERT is used to measure the bit error rate of a given channel at the "optimum sampling point" – an idealized setpoint in the middle of the eye. The resulting eye diagram is examined by means of a scope. The signal eye is checked against an on-screen reference hexagon. Matching the eye diagram with this hexagon requires a number of adjustments that typically take several minutes to complete.

Inherent disadvantages of this method:

•Slow because of the two-pass approach. Each individual eye diagram needs to undergo visual checking and a number of scope display adjustments to see whether or not the channel output is within specifications.

•This method analyzes one channel at a time, thus failing to account for cross-talk effects typical of "real-world" stress conditions under which multiple channels are active at the same time.

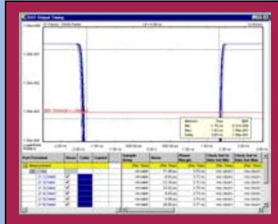
Verdict: **OK for R&D lab use still lacking for proper documentation, but far too slow and cumbersome for manufacturing applications.**

New Test Method in R&D

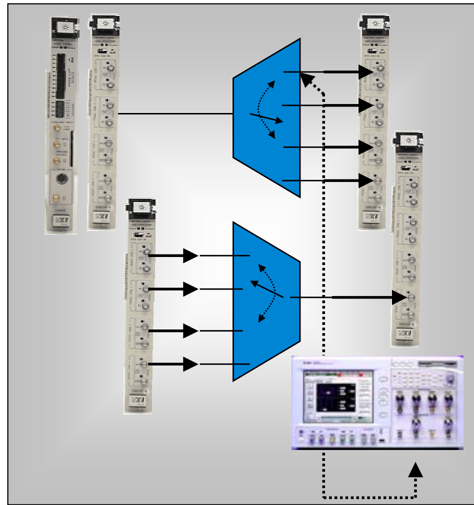
Mux/Demux Example

Major Improvement

BER, I/O Timing, Eye Opening



- **Individual test**
- **BER, Bathtub for Timing and Jitter on all channels**
- **Scope for Conformance**



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The new method combines two things:

1. All channels are stimulated and/or analyzed at the same time. The parallel outputs of the DEMUX go to an analyzer channel each thus doing BER measurement simultaneously: with the variable sampling point all channels can measure the output timing simultaneously also.

2. The measured points will be collected by the test controller and visualized ion form of the “bath tub measurement”. This measurement provide the data sheet values like ‘clock to data’ min/max (like setup/hold times) instantaneously.

The scope is still in use for analog type measurements , e.g. transition times.

Benefits:

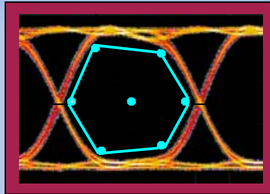
•Speed: **all channels of the DUT are stimulated and analyzed simultaneously, allowing all failure modes to be analyzed in a single pass.**

•Efficiency: **all channels are documented in one test. The visualization provides the required values as direct readout.**

New Test Method in Manufacturing

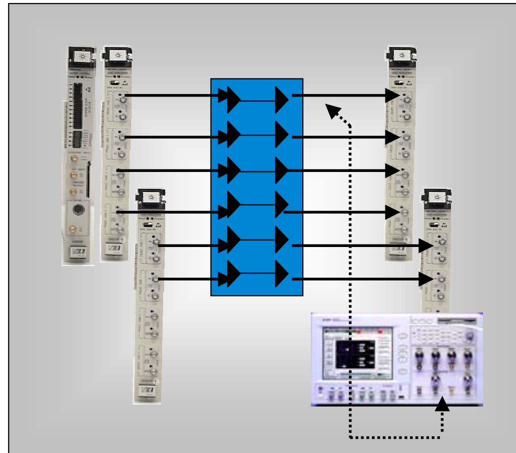
Multiple Optical Transceiver Example

Fast Eye Mask



- Very fast
- Filter: if marginal THEN use scope
- Selectable number of test points

Major Improvement



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The new method satisfies the performance prerequisites of the manufacturing arena **combining:**

1. The parallel BER **measurement performs stimulation and analysis simultaneously across a total of 60 lines (e.g. 30 stimulus and 30 response)**

2. The 'fast eye mask' speeds up channel testing by orders of magnitude. It returns a "part within spec" result in less than one second. To achieve this performance level, the following procedure is applied to all channels under test:

•The ParBERT analyzer finds the eye center point automatically.

•An offset procedure checks the BER for a test-specific number (1 – 32) of perimeter points which define the minimum area surrounding the eye diagram.

•The BER (Bit Error Rate) is compared against defined limits.

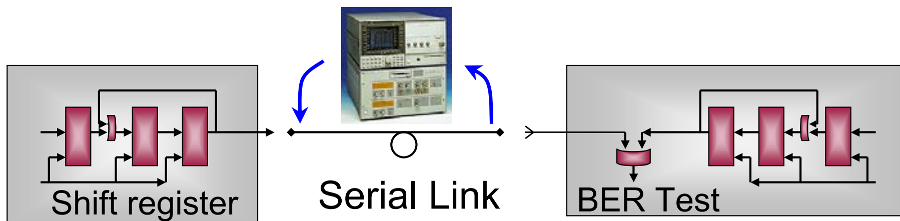
Benefits:

•Speed: **all channels of the DUT are stimulated and analyzed simultaneously, allowing all failure modes to be analyzed in a single pass.**

•Efficiency: **manual test engineer interaction is required "by exception" only; if a channel is found to be "out of spec", the eye diagram of that particular channel is flagged for further examination, e.g. by means of a scope.**

PRBS Data

(Pseudo Random Binary Sequence)



- PRBS: standardized
- Polynomial 2 ^n-1 & algorithm
- Stress by consecutive 1's and 0's
- Deterministic, predictable out of n bits
- Receiver synchronizes from incoming data

<u>What is PRBS</u>

For testing the physical layer, the industry uses the pseudo random binary sequence (PRBS). This is standardized by ANSI, ITU, and CCITT.

PRBS is defined by the polynomial 2^n-1 and a recurring algorithm. A shift register, with internal feedback defining the algorithm, is used for generating the stimulus data stream.

On the analyzer side, the same register with the same feedback is used. For a limited time, this will listen to the incoming data stream. It then starts to generate additional data that checks the incoming bits.

The future signal can be predicted by capturing the n bit failure-free data stream. Receivers can be synchronized for BER measurement from a running data stream. There is no need to know the start or synchronization signal from the stimulating side.

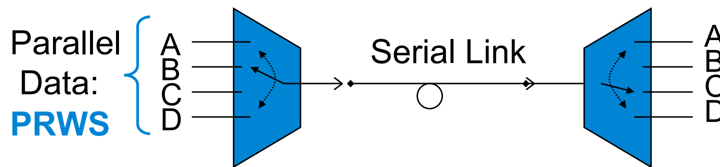
PRBS provides stress to the device under test (DUT) by a defined maximum number of consecutive '1's and '0's.

The Gigabit Ethernet community recommends the use of 2^7-1. The SONET/SDH community has standardized on the use of PRBS 2^23-1.

The higher the polynomial gets, the more consecutive '0's and '1's appear, stressing the clock recovery circuits. It is often desirable to extend the maximum number of same bits or to insert one or more errors into the bit stream. In this case, memory is needed because the shift register cannot do this job.

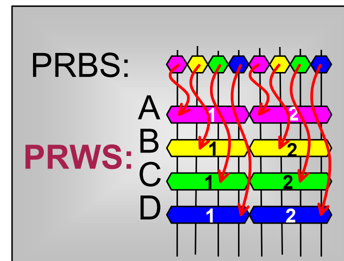
PRWS Data

(Pseudo Random Word Sequence)



PRWS is defined by:

- **Polynomial 2^n-1**
- **Algorithm**
- **Parallel bus width**



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<u>What is PRWS</u>

Pseudo random WORD sequence (PRWS) is an extension of PRBS.

It is defined by:

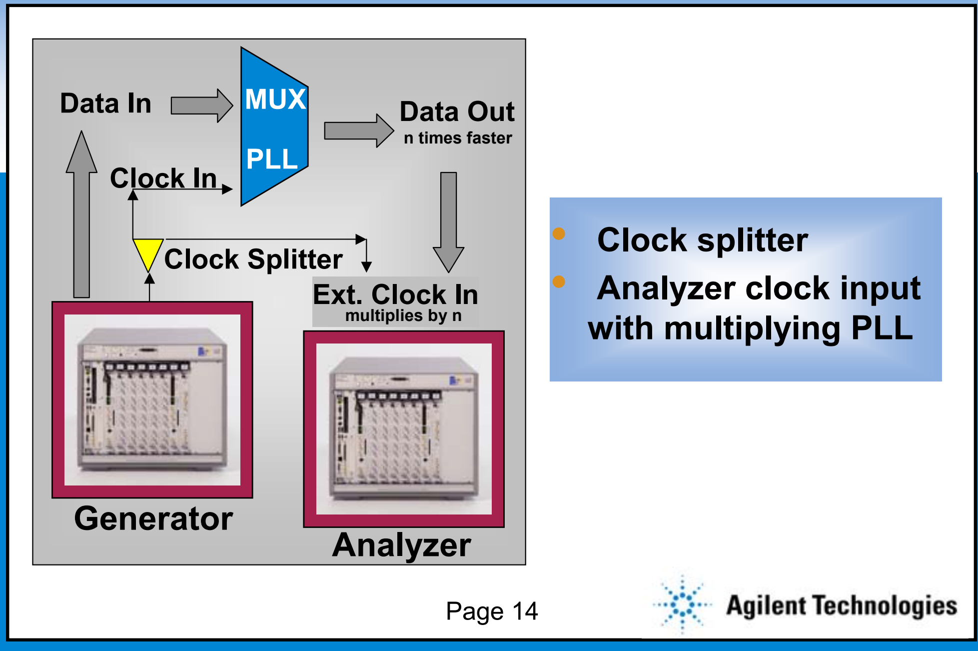
- **A polynomial 2^n-1**
- **An algorithm**
- **A parallel bus width**

The bits of the PRBS are assigned to parallel lines in the same way that multiplexing creates PRBS. Vice versa, PRBS applied to a DEMUX produces PRWS.

In principle, there are no limits to the port size on the parallel side. The PRWS can be generated from shift registers similar to the PRBS. There are only a few exceptions concerning port sizes and algorithms which are not possible.

For most polynomials in practical use (2^7-1, 2^23-1), there are only a few limitations. The benefit is a test system that handles PRBS and PRWS allowing BER testing:

- **Parallel to serial**
- **Serial to parallel**
- **Parallel to parallel**
- **Multiple serial to multiple serial**

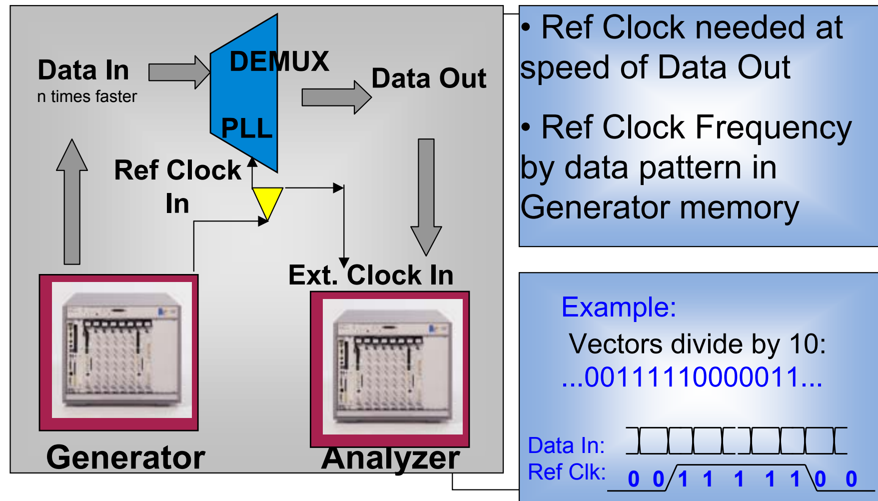


Now we talk about preparing a test system clock wise. As the MUX output runs n times faster, generator and analyzer need to run at different speeds. The constant phase relation between the two clocks is essential.

Ideally the analyzers would run on the same clock than is provided by the PLL inside the DUT to clock out the data at high speed. Unfortunately this clock is not available off-chip. So this clock has to be generated in the test system. This works with splitting the clock and feeding one part into the ext. clock input of the analyzer part. The PLL there takes care to multiply with the same factor than inside the MUX chip. This works pretty well as we can rely on the short term stability of the PLL circuitry.

(One should be aware that this principle works only if there are no long transmission paths involved. In this context, long transmissions in this term would be in µs or ms timeframes. Long transmission times occur if there is a longer fiber inside the DUT, or if there are wireless transmission sections. In this case, a clock recovery close to the input of the analyzers is required.)

Clock System, DEMUX with Reference Clock In



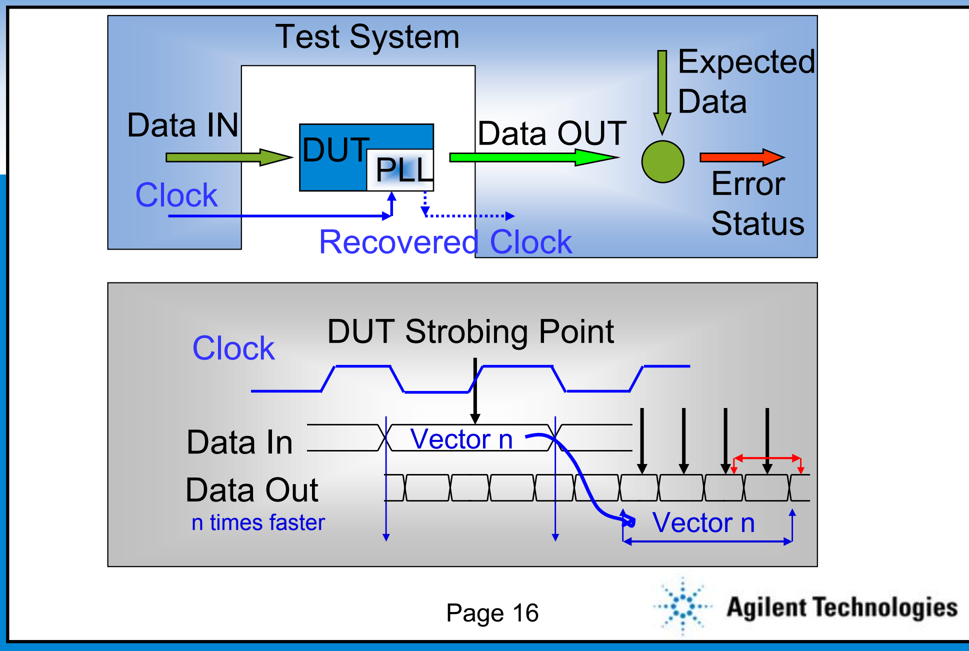
This is the example of the DEMUX which requires a reference clock.

This reference clock is at speed with the parallel side or even half speed there for ‘double pumped’ devices. So the generator has to deliver signals with two different speeds. One will be the high speed data, the other the low speed clock.

Such a clock channel can be established by using a pattern in memory which performs a ‘divide by n’. To do so a repetitive stream of n/2 times ‘1’s and n/2 times ‘0’s. as shown it the example here. This clock goes to the analyzer again. In case the device is ‘double pumped’, the PLL there has to multiply x2 again. But this also ensures the constant phase relation between the high speed data and the low speed clock.

Only with this clock the analyzer channels will correctly sample the data coming from the DUT (device under test).

If the DEMUX provides a recovered clock, this is the best choice to use it directly for the analyzer as ext. clock input.



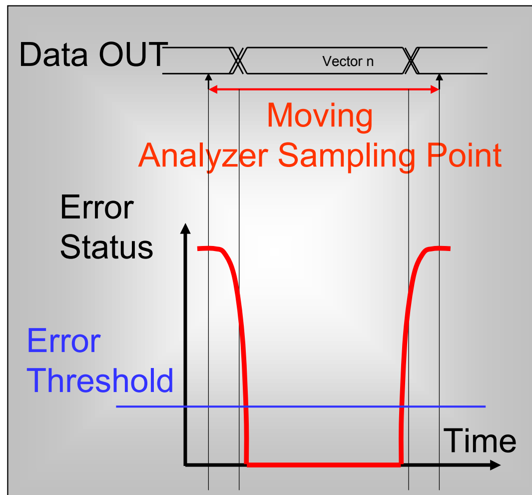
This example shows a MUX port. The MUX port receives a number of input signals timed by an input clock. On the output side there is no clock and the speed is a multiple of the original input signal. The bits supplied as a parallel vector to the input port now appear serialized within the data stream. This serialized frequency is a multiple of the input clock.

The position of the bits in the serial stream may not be fixed with reference to the input clock, because the initial position of the multiplexer's starting phase may be different at every power up.

On the output side, characterization depends on BER, 'eye opening' and jitter. Due to lack of stability in terms of design architecture, any relation from input to output is of minor interest for now.

To make 'eye opening' measurements on the output side, first, a test system must run at the speed of the data output. Second, the analyzers must synchronize to the proper bit phase. This was discussed more in detail in last year's paper, see reference [1] for details. When this synchronization has been achieved, the BER can be measured. Third with the capability of moving the s delay/sampling point around, the BER can be gathered as a function of sampling point position. Out of these data, the eye opening parameters can extracted. Even jitter measurements can be performed.

Multiple Bullet Levels



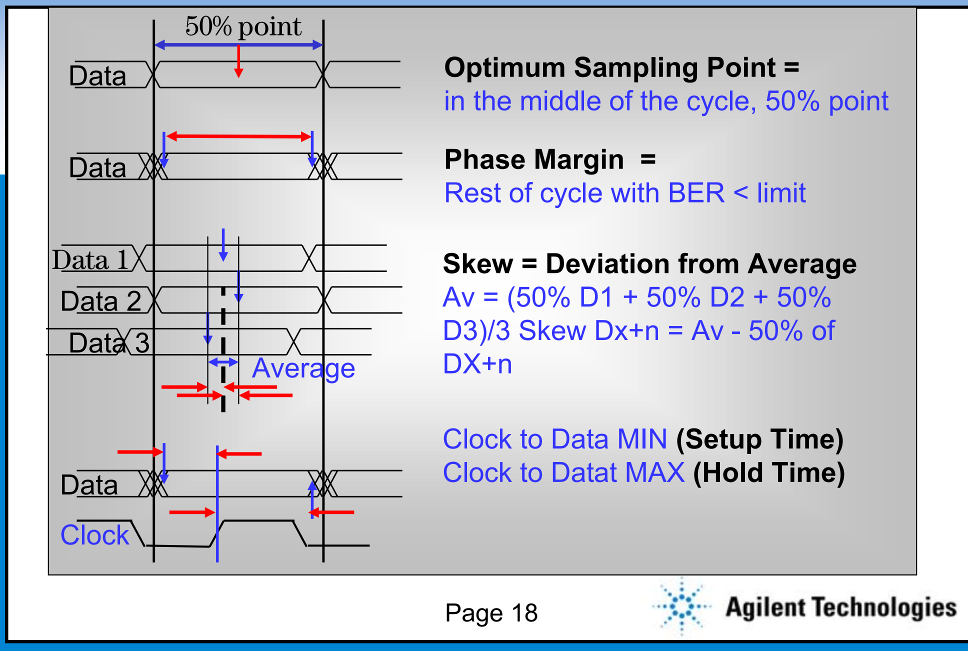
Timing Measurements:
-> Optimum Sampling Point
-> Skew
-> Phase Margin
-> Setup/Hold Time
-> Jitter

Again the important element in doing characterization is the ability to move timing edges around. A generator can delay stimulus signals with respect to each other. An analyzer allows the sampling point to shift.

Moving the sampling point during one cycle and plotting the error rate results in a graph called a ‘bathtub’. This graph shows ‘time’ on the x axis and a ‘BER’ figure on the y axis.

The name ‘bathtub’ results from the specific shape of the curve. This shape results from the BER figure getting lower; therefore, more test vectors must be processed. If the test runs are longer, the jitter band of a “real world” signal becomes wider.

Bathtub measurements are the basis for all measurements listed above including jitter measurements. In this case just one branch of the bathtub is evaluated. As long as the jitter is random, the result can be represented as an rms value. Otherwise it is represented as a pp (peak to peak) value.



This is the definition of 'output timing':

1. **The optimum sampling point occurs in the middle of a data cycle; it is also called the 50% point.**

   Using this point for sampling data provides the most margin against noise, jitter and other degradation mechanisms. A clock recovery circuit will automatically adjust the sampling for this point. But be aware that circuitry with an external clock may specify this as unsymmetrical because internal propagation delays between clock and data may be different.

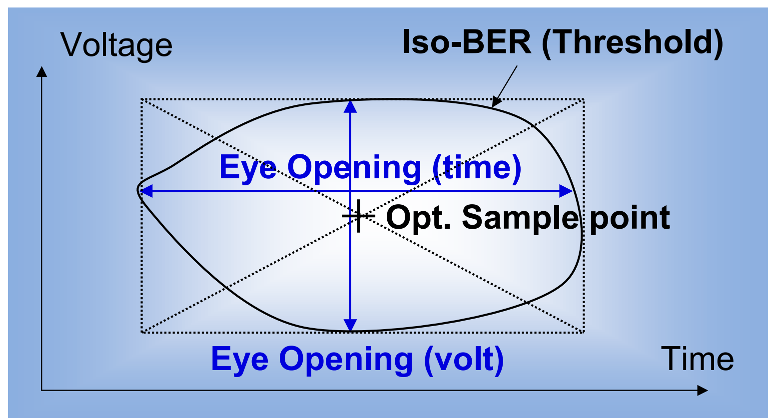
2. **Phase margin: Ideally, data will be stable for the full cycle. But because of finite transition times, duty cycle effects, and jitter, the window for stable data is less than one period. This window width is called phase margin.**

   Some effects--like jitter--are statistical in nature. Therefore, the phase margin is determined by how long a test will be done or how many test vectors are used. Duty cycle effects depend on the type of test vectors that are used.

3. **Skew: Individual lines on a bus may not switch on at the same time. Skew is defined as the deviation of the 50% point of the average over all bus lines.**

4. **Clock to Data min/max (Setup/Hold Time) is the time with reference to a clock signal edge. Together, both times are usually the same as the phase margin.**

Eye Opening Definitions



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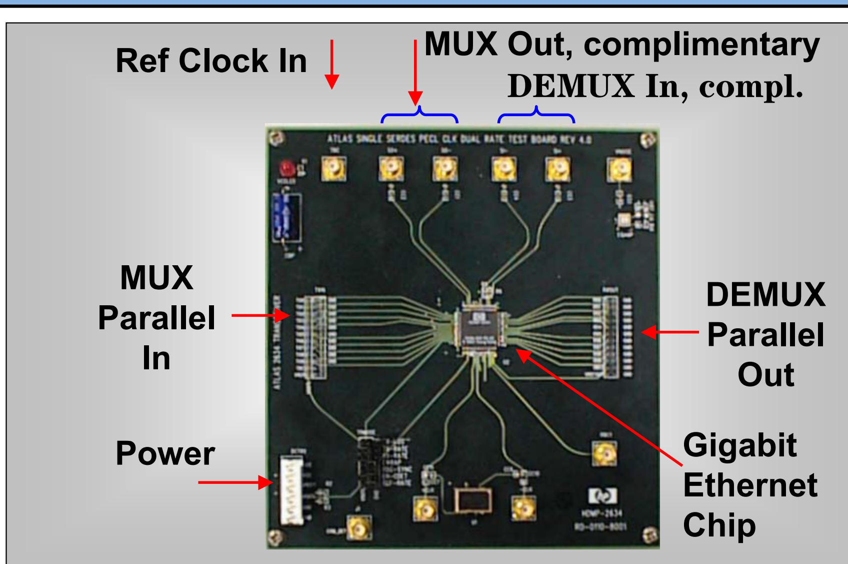
The ‘eye opening’ measurement is done in two dimensions: ‘time threshold’ and ‘voltage threshold’.

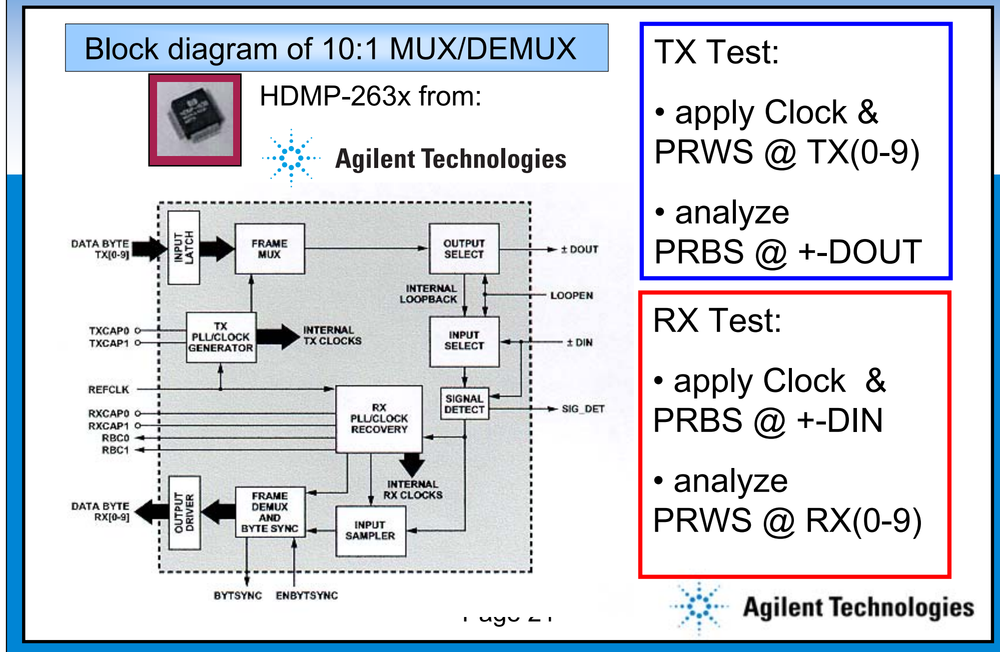
The ‘eye opening’ is defined as the maximum rectangle that can be put around an area with constant BER (ISO BER).

The intersection of the diagonals of this rectangle is defined as the ‘optimum sample point’.

Note that this is not necessarily the intersection of two lines which can be drawn for best ‘eye opening’ in terms of time and level!



Now taking another look at the Gigabit Ethernet Chip on the evaluation board, this slide shows all the connection points.



This slide shows a block diagram of the Gigabit Ethernet Chip from Agilent Technologies.

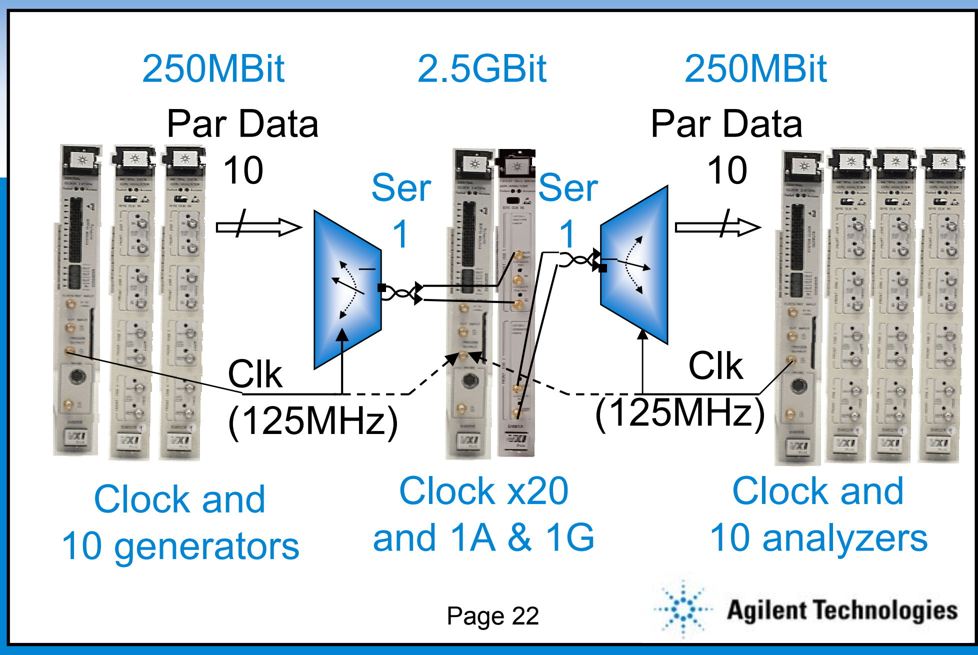
TX and RX are both in the same chip, so we can look at both parts consecutively.

TX test needs to apply clock and PRWS data to the inputs.

Dout and Ndout (+Dout, -Dout) will be compared with PRBS.

RX test needs to apply clock and PRBS at Din and nDin (+Din, -Din).

RX(0-9) will be compared with PRWS.



On this slide we see that:

• The device needs 250 MBit/s as a parallel data rate and a 125 MHz clock.

• The serial data rate is 2.5 GBit/s.

For analysis or generation of the serial side data, this clock group consists of a generator and analyzer.

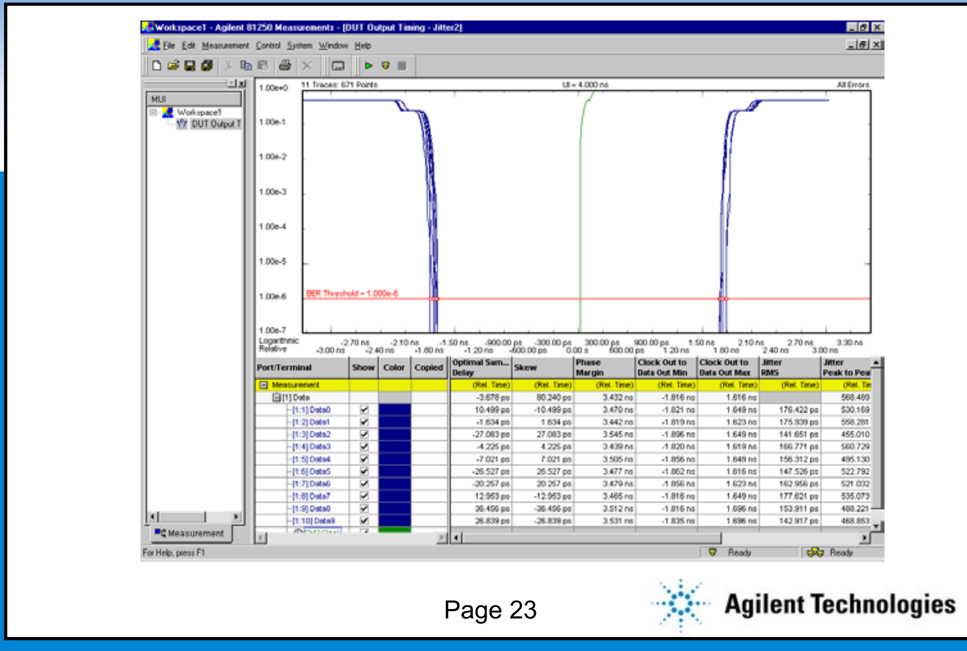
This component receives the 125 MHz clock and multiplies it internally by a factor of 20. The result is clock synchronous to 2.5 GBit/s.

The data synchronization is achieved by the bit synchronization capability of the sequencer.

The parallel side generates/analyzes PRWS (pseudo random WORD sequence) data.

The serial side will analyze/generate PRBS (pseudo random binary sequence) data.

Both sides will use the same polynomial.

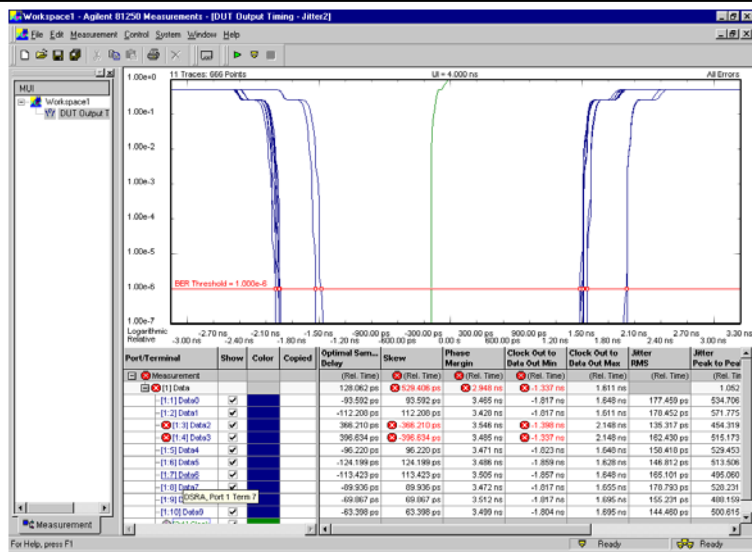


This is the ‘output timing’ measurement taken from the DEMUX:

blue is the 10 bit wide port, green is the clock reference slope, red is the BER threshold, which can be set by the user.

In the table of the bottom part you get all the parameters listed for each data output (Data0 ..Data9) and overall for the port (Data).

DEMUX Output Timing Result (2)



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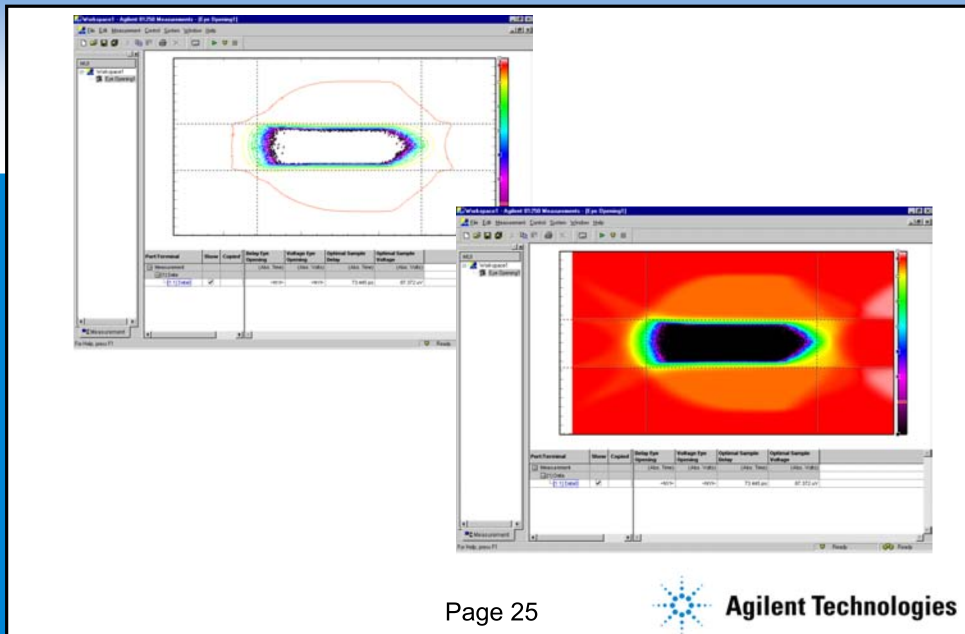
This is the ‘bathtub’ measurement with Pass/Fail enabled. Here we have two data lines with excessive skew.

With the PASS/FAIL capability there is a limit set for each parameter. If once a data line exceeds this limit, the parameter is flagged with red.

MUX Eye Opening Result



The 'eye opening' at the MUX output is visualized with :

- **Contour plot**
- **Pseudo color plot**
- **there is also a equal BER representation (not shown here) which allows to overlay several signals**
- **there are markers for 'time' and 'threshold'**

MUX Fast Eye Mask Result

Fast Eye Mask Measurement (1-32 Points)

1 - 8 Pts Del (%)	Offs (V)	9 - 16 Pts Del (%)	Offs (V)	17 - 24 Pts Del (%)	Offs (V)	25 - 32 Pts Del (%)	Offs (V)
-0.5	0	0	0	0	0	0	0
0.5	0	0	0	0	0	0	0
-0.16	0.3	0	0	0	0	0	0
0.16	0.3	0	0	0	0	0	0
-0.16	-0.3	0	0	0	0	0	0
0.16	-0.3	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Bit Error Rates

Pts.	Error Rates
1	** 5.000170e-001
2	0.000000e+000
3	0.000000e+000
4	0.000000e+000
5	0.000000e+000
6	0.000000e+000

Number of Pts. 6
Port Number 1
Terminal Number 1
Max Compared Bits 1000000
Max Errors 1000000
System Name DSRA
Pass/Fail Criteria 1e-006 (BER)
Measurement State STOPPED
Measure
Close

Fast Eye Mask:

- Predefined points (1 . . 32) by delay & threshold offset
- 6-Point-Measurement 1 sec typically

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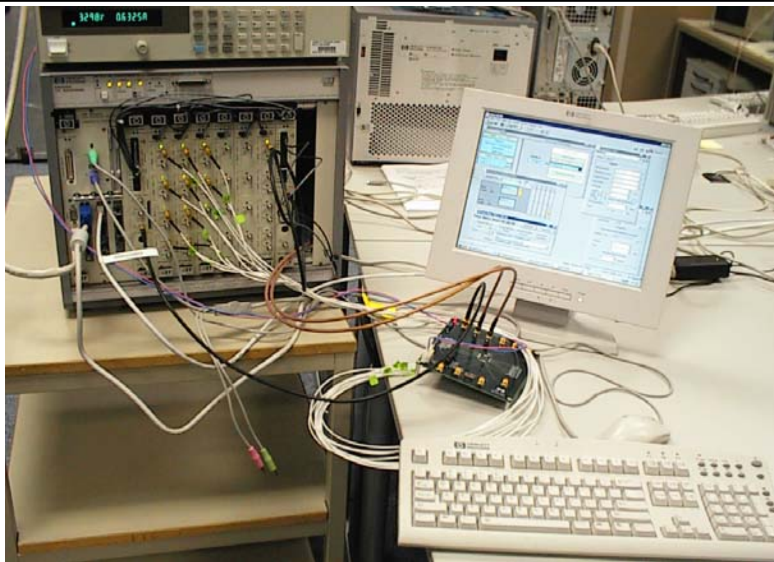
The fastest way to check the ‘eye opening’ is to check the BER at ‘n’ different points within the eye. Using 6 points comes close to the ‘hexagon’ type measurement done with a scope.

The points and the limits for the BER are both defined and the measurements function returns a Pass/Fail result.

This measurement function is triggered by remote control. The returned Pass/Fail information tells the robotics to separate the good parts from the bad parts.

System Configuration in Actual



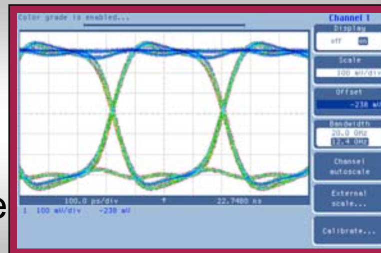
This is the ParBERT 81250 connected to Gigabit Ethernet evaluation board.

It contains 10 generator/analyzers (660) for the parallel interface and 1 generator/analyzer for the 2.5GBit/s.

Conclusions: R&D vs. Manufacturing

Design Issues:

Eye Opening
Output Timing



-> need to test the same but:

R&D:
- characterization
  - Iso BER
  - Skew
  - jitter

Manufacturing:
- meet the spec
- “good enough”
- fast, throughput

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Both R&D and manufacturing have to test for the same timing parameters. But their purpose for testing is totally different:

R&D **wants to know where the limits and the margins are. Their main question is: How well does the device work?**

This kind of testing is called ‘characterization’. Because a lot of measurements, which depend on other parameters, have to be performed, it is a time-consuming task. The parameters of interest include a long list, ISO BER, skew and jitter are just some samples.

The ‘parallel BER testing method’, together with the visualization of the ‘timing’ measurement, provides all the parameters as a direct read-out for the R&D engineer.

Manufacturing **has to verify spec. compliance of each individual part. As throughput is essential, they have to measure the same parameters as R&D. However, their methodology is different.**

The issue is to determine, as quickly as possible, whether or not the individual parts meet the specification.

Here the ‘parallel BER testing method’ together with the ‘fast eye mask’ measurement is the key for speed-up the measurements.